C-V ANALYSIS AT VARIABLE FREQUENCY OF MOS STRUCTURES WITH DIFFERENT GATES, CONTAINING Hf-DOPED TA₂O₅

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Abstract. The quality of the interface between the insulating layer and the Si substrate in contemporary submicron MOS technology is a critical issue for device functioning. It is characterized through the electrically active defect centers, known as interface states. Their response to the frequency is discussed here, by analyzing capacitance-voltage and conductance-voltage curves. The C-V method is preferred in many cases, since it offers easy measurement, and it is applied to extract information about interface traps and fixed oxide charge, at different frequencies. This technique, related with frequency dependent G-V measurements, can be very useful in characterizing charge trapped in the dielectric and at the interface with Si. By extracting the value of frequency dependent flatband voltage, we have obtained the fixed oxide charges at flatband condition. A comparison between the results obtained by two different methods is made. The samples that are studied are metal-insulator-semiconductor (MIS) structures that include high-κ dielectric as insulating layer (Hf doped Ta₂O₅), with thickness of 8 nm, with different metal used as gate electrode. Here the influence of the top electrode on the generation and behavior of the traps in the oxide layer is discussed. The results show that the value of metal work function of the gate material is an issue that should be considered very carefully, especially in the case of high work function metal gates, when generation of extra positive charge than in the case of other metals is observed.

PACS: 68.55.-a; 61.43.Dq

1. INTRODUCTION

The introduction of high-κ materials as a replacement of SiO₂ in various microelectronic applications requires profound knowledge of the properties of high-κ dielectric materials, especially the properties related with certain applications, for which high-κ candidates have proved themselves as most suitable dielectrics. Among them Ta and Hf oxides meet the requirements for application in dynamic random access memories (DRAM’s) and MOSFET’s, respectively [1,2]. Pure Ta₂O₅, with its high storage ability (i.e. high permittivity in combination
with high breakdown field) and low leakage current is studied in detail. The main drawbacks of 
Ta₂O₅, identified as its thermodynamic instability on contact with Si, which leads to the 
formation of lower-\(k\) interfacial layer and its relatively small bandgap (4–4.5 eV), which defines 
small barrier heights for carrier injection, hence increased leakage current, are tailored by 
doping of Ta₂O₅ with a proper element or by mixing it with another oxide. It is shown [3] that 
this approach indeed could extend the potential of pure Ta₂O₅ as a high-\(k\) material, because the 
process of mixing HfO₂ and Ta₂O₅ modifies the dominant conducting mechanisms and changes 
the traps parameters as compared with pure Ta₂O₅ stacks with the same high-\(k\) dielectric 
thickness.

The aspect of the influence of top metal electrode on electric parameters of the devices 
with high-\(k\) material [4–6], especially on the evolution of degradation mechanisms and 
generation and behavior of bulk and interfacial traps, uncovers a lot of unsolved problems that 
require further studying. This especially refers to the metals with higher value of work function 
when used as gate electrodes on doped high-\(k\) structures.

2. EXPERIMENTAL

Chemically cleaned p-type (100) Si wafers with resistivity of 15 \(\Omega\)cm were used as 
substrates. Tantalum oxide was deposited by reactive sputtering of a Ta target in an Ar + 10% 
O₂ atmosphere obtaining Ta₂O₅ layer approximately 7.5 nm thick; the working gas pressure was 
0.33 Pa and rf power density was 3.6 W/cm². The Si substrate was heated at 200 °C during 
deposition. The Hf-doped Ta₂O₅ layers were obtained by deposition of Hf layer ~ 0.7 nm thick 
on the top of previously deposited Ta₂O₅ layer. Hf was deposited by sputtering of a Hf target in 
an Ar atmosphere. The samples were subjected to a post-deposition annealing at 400°C in N₂ for 
30 min in order to mix the two layers and to ensure the diffusion of Hf into the matrix of Ta₂O₅, 
resulting in an 8 nm thick final layer. Top electrodes of MOS structures were formed by 
sputtering of TiN, Mo, Pt and Ta in an Ar atmosphere. Fabrication sequence ended with post 
metallization annealing in forming gas at 450 °C for 1 h.

The samples were studied by means of \(C-V\) measurements, at different frequencies 
50 kHz, 100 kHz, 200 kHz, 500 kHz and 1 MHz, which means that the structures are tested both 
under low and high frequency conditions. From these measurements frequency dependence of 
the value of flatband voltage and fixed oxide charges is observed. For determining these values, 
also, the \(G-V\) method was used. The results obtained by these two different methods are 
compared.

3. RESULTS AND DISCUSSION

When a MOS structure is in the depletion region, applying small ac signal causes 
ocillations of the Fermi level around the mean position governed by the dc bias. In these 
conditions the presence of interfacial states and their response to the measurement, changes the 
value of measured capacitance. It can be seen from the Fig. 1 that at low frequencies, the values
of capacitance of all studied structures that contain different metal gates, are higher than at high frequencies. The higher values of capacitance at low frequencies are due to excess capacitance resulting from the interface states in equilibrium with the Si-substrate that can follow the ac signal. This observation has been attributed to the capacitive response of interface states to the measurement in the case of silicon dioxide insulating layers [7] and also was observed in the case of Ta2O5 thin films [8]. At high frequencies the charges at the interface states cannot follow an ac signal, making no (or negligibly small) contribution of interface capacitance to the total capacitance. In the case of stacked high-\textit{k}/ SiO2 dielectric layers, the contribution of the border traps to the capacitance, also, has to be taken into account [9]. Since we study Ta2O5:Hf/SiO2 dielectrics, it is expected that the contribution of the border traps in the Ta2O5:Hf layer, will be significant, which is confirmed by the measurement.

Fig. 1: Frequency dispersion of \textit{C-V} curves of Ta2O5:Hf/SiO2/Si structure, with a) Mo; b) Pt; c) Ta and d) TiN as top electrode. The capacitance alteration is measured in both directions, i.e. this represents the hysteresis of \textit{C-V} curves.
For all samples from the obtained C-V curves, lowest values of capacitance in accumulation at the highest frequencies (1 MHz) were obtained (Fig.1). This observation is the same as in the case of pure Ta$_2$O$_5$, Hf doped Ta$_2$O$_5$ with Al gate and also it is observed here, in the case of Hf doped Ta$_2$O$_5$ samples with different gate electrodes (Mo, Pt, Ta and TiN). The observed hysteresis was negligible, leading to very low slow states density of the order of $10^{10}$ cm$^{-2}$.

From C-V curves and using the method of extraction of the values of capacitance in accumulation [10], we have obtained the values of flatband voltage and fixed oxide charges, using the standard capacitance method [11,12]. Flatband voltage is the voltage corresponding to the value of flatband capacitance ($C_{fb}$), calculated according to the equation (1):

$$C_{fb} = \frac{C_{acc} \varepsilon_s A}{C_{acc} + \frac{\varepsilon_s A}{\lambda}},$$

where $C_{acc}$ is the capacitance in accumulation, $\varepsilon_s$ is the permittivity of the substrate material (Si), $A$ is the gate area and $\lambda$ is the extrinsic Debye length, as calculated by:

$$\lambda = \sqrt{\frac{\varepsilon_s kT}{q N_a}},$$

where $kT$ is the thermal energy at room temperature, $q$ is the electron charge and $N_a$ is the acceptor concentration in silicon. If the value of $N_a$ is not given by the manufacturer of the substrate, it can be calculated by plotting the voltage dependence of $1/C^2$ [11,12], given by the following expression

$$\frac{\partial (1/C^2)}{\partial U} = \frac{2}{q \varepsilon_0 \varepsilon_s N_a A^2}.$$

The acceptor concentration is calculated from the slope of this plot, as presented at Fig. 2. Once the value of $C_{fb}$ is known, the value of $V_{fb}$ can be obtained from the C-V curve data, by interpolating between the closest gate-to-substrate voltage values.

Fixed oxide charges $Q_{ox}$ for samples with different metal gates were determined, using the equation

$$V_{fb} - W_{MS} = \frac{Q_{ox}}{C_{acc}},$$

where $V_{fb}$ is the flatband voltage, $W_{MS}$ is the metal-semiconductor work function, and $C_{acc}$ is the oxide capacitance. The values of metal work functions for Mo, TiN, Pt and Ta taken from literature are as follows, 4.2 eV, 4.7 eV, 5.6 eV and 4.25 eV, respectively. The obtained surface densities of the fixed charges, for samples with various gates, calculated using flatband voltage values obtained by C-V curves, are presented in Table 1.
Fig. 2: Extraction of the acceptor concentration \( N_a \) of the substrate from \( C-V \) curves of Ta\(_2\)O\(_5\):Hf/SiO\(_2\)/Si structure, with Mo, Pt, Ta and TiN as top electrode.

The presence of the interface states is evident also by their influence on the measured conductance at different frequencies (Fig. 3). Here, same as in the case of frequency dependence of \( C-V \) curves, there isn’t any dependence of the metal used as a gate, because the frequency dependence of capacitance, as well as of conductance is due to the interfacial charges, present at the interface of the insulating layer (in this case doped Ta\(_2\)O\(_5\) and intermediate SiO\(_2\)) and the Si substrate. The quality of this interface is the same for all samples, since they belong to the same manufacturing sequence, and only differ in the deposited top metal gate. \( G/\omega-V \) curves give a pick, which is positioned at the flatband voltage. Such behavior of the \( G/\omega \) peaks is attributed to particular distribution of surface states between Si/oxide interface [13]. Using this fact, we will extract the values of flatband voltage also from \( G/\omega-V \) curves, in order to make a comparison between these two methods. These values are also presented in Table 1.

From the values presented in Table 1, it can be seen that both methods give very similar values of flatband voltage. These values show tendency to increase with the rise of the measuring frequency. This shift of flatband voltage toward higher values is due to the response of interfacial states at the interface oxide/Si substrate, that at lower frequencies contribute in the overall capacitance of the structure, which is not the case at higher frequencies. Here the influence of the gate electrode becomes obvious, since it is also included in the definition of the value of flatband voltage by equation (4). Flatband voltage for samples with Mo, Ta and TiN gate (which have similar values metal work function) are close to each other, while in the case of Pt (gate with highest work function) different values of flatband voltage are obtained.

Also it can be seen that the calculated values of oxide charges for Mo, Ta and TiN are similar, while for Pt gate it is substantially higher, i.e. in these samples an extra positive charge exists. This observation is related with the nature of the interface at the contact between the oxide and the gate. In the case of high work function metal, the position of metal Fermi level favors the transition of electrons from the oxide layer into metal conduction band, thus leaving uncompensated positive charge in the interfacial region. The presence of this extra positive
charge is registered in our calculations, too, whose values as presented in Table 1 are almost one order of magnitude higher than in the case of other gates, which are not labeled as high work function metals.

**Fig. 3:** Frequency dispersion of $G/\omega$-V curves of $\text{Ta}_2\text{O}_5$:$\text{Hf}/\text{SiO}_2$/Si structure, with a) Mo; b) Pt; c) Ta and d) TiN as top electrode. The pick position corresponds to the value of flatband voltage.

**Table 1** Extracted values of flatband voltage and fixed oxide charges from two different methods, from $C$-$V$ curves and from the peack position of $G/\omega$-V curves

<table>
<thead>
<tr>
<th>$f$ (kHz)</th>
<th>$C_{ac}(\text{pF})$</th>
<th>$C_{af}(\text{pF})$</th>
<th>$U_{fb}$ (V)</th>
<th>$Q_{ox} (\text{C/cm}^2) \times 10^{11}$</th>
<th>$U_{fb}$ (V)</th>
<th>$Q_{ox} (\text{C/cm}^2) \times 10^{11}$</th>
<th>$U_{fb}$ (V)</th>
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<tbody>
<tr>
<td>TiN</td>
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<tr>
<td>50</td>
<td>1960</td>
<td>286</td>
<td><strong>0.32</strong></td>
<td>5.88</td>
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<td>2050</td>
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<tr>
<td>100</td>
<td>1929</td>
<td>286</td>
<td><strong>0.35</strong></td>
<td>7.23</td>
<td><strong>0.42</strong></td>
<td>1760</td>
<td>282</td>
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<tr>
<td>200</td>
<td>1826</td>
<td>283</td>
<td><strong>0.38</strong></td>
<td>8.22</td>
<td><strong>0.49</strong></td>
<td>1100</td>
<td>257</td>
</tr>
<tr>
<td>500</td>
<td>1353</td>
<td>269</td>
<td><strong>0.42</strong></td>
<td>7.44</td>
<td><strong>0.52</strong></td>
<td>1030</td>
<td>253</td>
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<tr>
<td>Ta</td>
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<td>50</td>
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### 4. CONCLUSION

In this paper we have characterized samples that contain Hf doped Ta$_2$O$_5$, alternative dielectric, marked as high-$k$ material. Here we analyze the quality of the interfaces of this multilayered structure, the interface between oxide/Si substrate and metal/oxide interface. The presence of interfacial electrically active states is confirmed by their response to the measuring frequency, and therefore their influence to the flatband voltage. These values are calculated using both $C$-$V$ and $G/\omega$-$V$ measurements, which converges toward similar values. The influence of the metal gate is strongest in the case of high work function metal, which leads to the creation of extra positive charges. These positive states are responsible for other phenomena, like charge trapping observed in the case of high work function metal gate, which is out of the scope of this paper.
Acknowledgement

This work was supported by Macedonian Ministry of Education and Sciences under contract No. 13-3573 and by Bulgarian National Science Foundation under contract DTK 02/50.

REFERENCES


